

Notice of References Cited

Application/Control No.

09/721,152

Applicant(s)/Patent Under
Reexamination
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Examiner

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Art Unit

2183

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U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-5,922,065	07-1999	Hull et al.	712/24
	B	US-6,457,173	09-2002	Gupta et al.	717/149
	C	US-			
	D	US-			
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	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Petrov, "Code Compaction and Parallelization for VLIW/DSP Chip Architectures," June 1999, pp.38-40
	V	Aditya et al., "Automatic Design of VLIW and EPIC Instruction Formats," April 2000, pp. 71-82
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.